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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/898,386 | 07/05/2001 | Shui-Hung Chen | TS00-424 | 3633 |

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| EXAMINER |
|---|
| NADAV, ORI |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 01/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/898,386 | CHEN ET AL. | |
| | Examiner | Art Unit | |
| | ori nadav | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (6,011,681) in view of Chen et al. (6,016,002).

Ker et al. teach in figure 8 an electrostatic discharge protection device comprising: a p region of a semiconductor substrate; an n+ region in the p region wherein the n+ region is connected to a first voltage supply Vdd1; an n-well region in the p region wherein the n+ region is spaced from the n-well region a distance such that a depletion region extends therebetween during normal operation; and a p+ region in the n-well region wherein the p+ region is connected to a second voltage supply Vdd2 of greater value than the first voltage supply during the normal operation wherein current is conducted through the n+ region to the p+ region during an electrostatic discharge event.

Although Ker et al. do not explicitly state that the n+ region is spaced from the n-well region a distance such that a depletion region extends therebetween during normal operation, this feature is inherent in Ker et al.'s device, because Ker et al.'s structure is

identical to the claimed structure. In the alternative, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the n+ region spaced from the n-well region a distance such that a depletion region extends therebetween during normal operation in Ker et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Ker et al. do not an n-well ESD device formed in a p-well region.

Chen et al teach in figure 4 an p-well ESD device formed in a n-well region 98.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Ker et al.'s device in a p-well in order to provide better electrical isolation for the device and because it is conventional to reverse the polarity of the transistor, respectively.

Regarding claims 2, 9 and 15, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a p-well region comprises a dopant concentration of between about 1xE15 atoms/cm3 and 1xE16 atoms/cm' in Ker et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 3, 10 and 16, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an n-well region comprises a dopant concentration of between about 5xE15 atoms/cm3 and 5xE16 atoms/cm3 and a junction depth of between about 0.3 microns and 1.0 microns in Ker et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 4, 11 and 17, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an n+ region comprises a dopant concentration of between about 1xE20 atoms/cm' and 1xE22 atoms/cm3 and a junction depth of between about 0.1 microns and 0.3 microns in Ker et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 5, 8 and 18, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a distance between the n+ region and the n-well region between about 0.2 microns and 1.0 microns in Ker et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 6-7, 12-13 and 19-20, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first and second voltage supplies is between about 1.0 Volts and 5.0 Volts referenced to the p-well region during the normal operation in Ker et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claim 14, Ker et al. teach in figure 8 a ground pad Vss2 connected to an external ground reference and to a p+ region in the p substrate.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al.

Chen et al. teach in figure 2 an electrostatic discharge protection device comprising: a p region 42 of a semiconductor substrate; an n+ region 54 in the p region wherein the n+ region is connected to a first voltage supply 60, an n-well region 44 in the p region wherein the n+ region is spaced from the n-well region a distance such that a depletion region extends therebetween during normal operation; and a p+ region 48 in the n-well region wherein the p+ region is connected to a second voltage supply 50 of greater value than the first voltage supply during the normal operation wherein current is

conducted through the n+ region to the p+ region during an electrostatic discharge event.

Although Chen et al. do not explicitly state that the n+ region is spaced from the n-well region a distance such that a depletion region extends therebetween during normal operation, this feature is inherent in Chen et al.'s device, because Chen et al.'s structure is identical to the claimed structure. In the alternative, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the n+ region spaced from the n-well region a distance such that a depletion region extends therebetween during normal operation in Chen et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Chen et al. do not teach in figure 2 an n-well ESD device formed in a p-well region. Chen et al teach in figure 4 an p-well ESD device formed in a n-well region 98.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Chen et al.'s device in a p-well in order to provide better electrical isolation for the device and because it is conventional to reverse the polarity of the transistor, respectively.

Regarding claims 2, 9 and 15, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a p-well region comprises a dopant

concentration of between about 1xE15 atoms/cm3 and 1xE16 atoms/cm' in Chen et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 3, 10 and 16, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an n-well region comprises a dopant concentration of between about 5xE15 atoms/cm3 and 5xE16 atoms/cm3 and a junction depth of between about 0.3 microns and 1.0 microns in Chen et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 4, 11 and 17, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an n+ region comprises a dopant concentration of between about 1xE20 atoms/cm' and 1xE22 atoms/cm3 and a junction depth of between about 0.1 microns and 0.3 microns in Chen et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 5, 8 and 18, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a distance between the n+ region

and the n-well region between about 0.2 microns and 1.0 microns in Chen et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 6-7, 12-13 and 19-20, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first and second voltage supplies is between about 1.0 Volts and 5.0 Volts referenced to the p-well region during the normal operation in Chen et al.'s device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claim 14, Chen et al. teach in figure 2 a ground pad 60 connected to an external ground reference and to a p+ region 58 in the p substrate.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B and N are cited as being related to ESD devices.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav

January 22, 2002

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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